Integrated Circuit Systems, Inc.

16-Bit Integrated Clock-LUT-DAC

General Description

The ICS5340 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262,144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contains 8 frequencies, 6 of which are programmable by the user. The memory clock has two programmable frequency locations.

The three 8-bit DACs on the ICS5340 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and V_{DD} ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

ICS is the world leader in all aspects of frequency (clock) generation for graphics, using patented techniques to produce low jitter video timing.
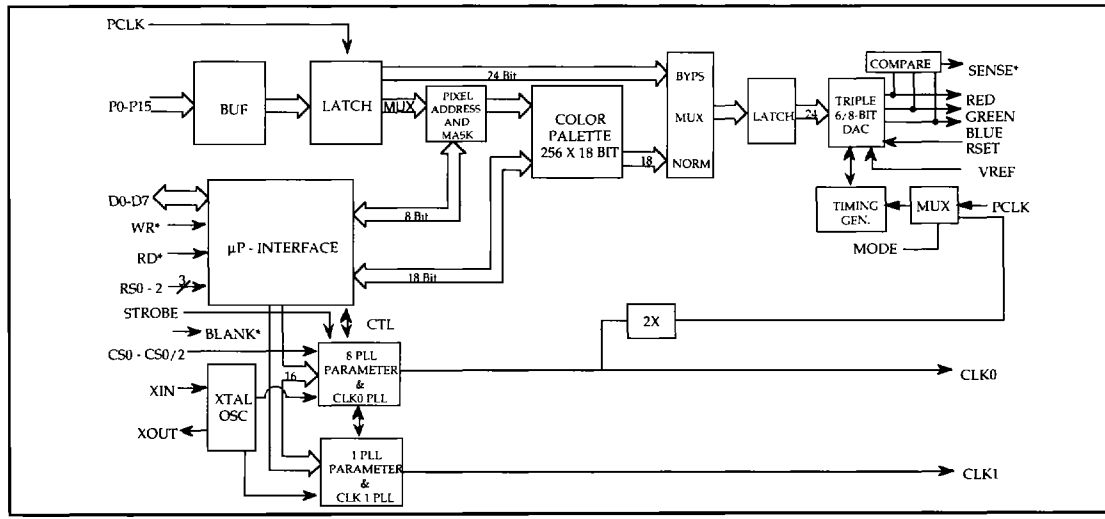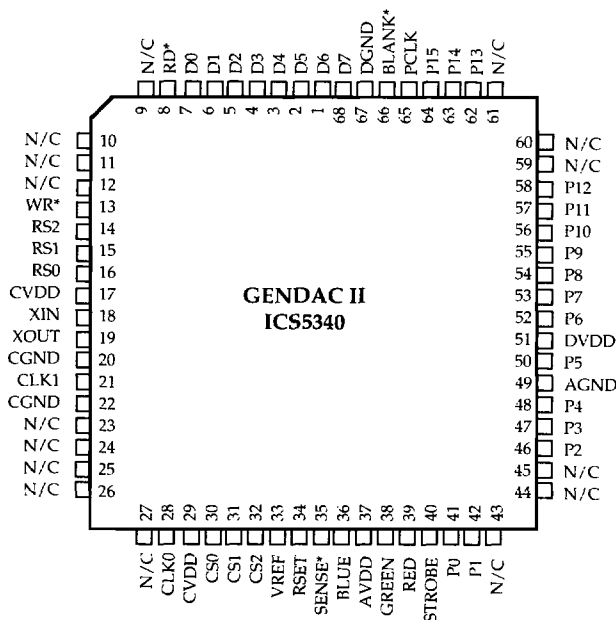
Features

- Triple video DAC, dual clock generator, and a color palette
- 24, 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGA modes
- High speed 256 x 18 color palette (135 MHz) with bypass mode and 8-bit DACs
- Two fixed, six programmable video (pixel) clock frequencies (CLK0)
- Two programmable memory (controller) clock frequency (CLK1)
- DAC power down in blanking mode
- Anti-sparkle circuitry
- On-chip loop filters reduce external components
- Standard CPU interface
- Single external crystal (typically 14.318 MHz)
- Monitor Sense
- Internal voltage reference
- 135 MHz (-3), 110 MHz (-2) & 80 MHz (-1) versions
- Very low clock jitter
- Latched frequency control pin

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Block Diagram

Pin Configuration

GENDAC II
ICS5340

Rev 1.0

Pin Description (68 pin PLCC) K-10

Symbol	Pin #	Type	Description
D7 - D0	68, 1 - 7	I/O	System data bus I/O. These bidirectional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.
RD*	8	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
WR*	13	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RS2	14	Input	Register Address Select 0. These inputs control the selection of one of the
RS1	15	Input	six internal registers. They are sampled on the falling edge of the active
RS0	16	Input	enable signal (RD* or WR*).
CVDD	17	-	Crystal oscillator and CLK0 power supply connect to AVDD.
XIN	18	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	19	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
CGND	20	-	VSS for CLK0. Connect to ground.

Pin Description (continued)

Symbol	Pin #	Type	Description
CLK1	21	Output	Memory clock output. Used to time the video memory.
CGND	22	-	VSS for CLK1. Connect to ground.
CLK0	28	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CVDD	29	-	CLK1 Power Supply. Connect to AVDD.
CS0	30	Input	Clock select 0. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS1	31	Input	Clock select 1. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS2	32	Input	Clock select 2. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
VREF	33	I/O	Internal Reference Voltage. Normally connects to a 0.1μ cap to ground. To use an external Vref, connect a 1.235V reference to this pin.
RSET	34	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
SENSE*	35	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
AVDD	37	-	DAC power supply. Connect to AVDD.
BLUE	36	Output	Color Signals. These three signals are the DACs' analog outputs. Each
GREEN	38	Output	DAC is composed of several current sources. The outputs of each of the
RED	39	Output	sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
STROBE	40	Input	Latches the input clock select signals CS0 - CS2.
P0 - P15	41- 42 46-48, 50	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
AGND	49	-	DAC Ground. Connect to ground.
DVDD	51	-	Digital power supply.
PCLK	65 52-58, 62-64	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address and BLANK* inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
BLANK*	66	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
DGND	67	-	Digital Ground. Connect to ground.

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Internal Registers

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
				There is a single Pixel Address register within the GENDAC. This register can be accessed through either register address 0,0,0 or register address 0,1,1. A read from address 0,0,0 is identical to a read from address 0,1,1.
				Writing a value to address 0,0,0 performs the following operations: a) Specifies an address within the color palette RAM. b) Initializes the Color Value register.
				Writing a value to address 0,1,1 performs the following operations: a) Specifies an address within the color palette RAM. b) Loads the Color Value register with the contents of the location in the addressed RAM palette and then increments the Pixel Address register.
0	0	0	Pixel Address WRITE	Writing to this 8-bit register is performed prior to writing one or more color values to the color palette RAM.
0	1	1	Pixel Address READ	Writing to this 8-bit register is performed prior to reading one or more color values from the color palette RAM.
0	0	1	Color Value	The 18-bit Color Value register acts as a buffer between the microprocessor interface and the color palette. Using a three bytes transfer sequence allows a value to be read from or written to this register. When a byte is read, the color value is contained in the least significant 6 bits , D0-D5 (the most significant 2 bits are set to zero). When writing a byte, the same 6 bits are used. When reading or writing, data is transferred in the same order - the red byte first, then green, then blue. Each transfer between the Color Value register and the color palette replaces the normal pixel mapping operations of the GENDAC for a single pixel.
				After writing three definitions to this register, its contents are written to the location in the color palette RAM specified by the Pixel Address register, and the Pixel Address register increments.
				After reading three definitions from this register, the contents of the location in the color palette RAM specified by the Pixel Address registers are copied into the Color Value register, and the Pixel Address register increments.
0	1	0	Pixel Mask	The 8-bit Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P0-P7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the microprocessor interface when the palette RAM is being accessed.

Internal Registers (continued)

RS2	RS1	RS0	Register Name	Description (all registers can be written to and read from)
1	0	0	PLL Address WRITE	Writing to this 8-bit register is performed prior to writing one or more PLL programming values to the PLL Parameter register.
1	1	1	PLL Address READ	Writing to this 8-bit register is performed prior to reading one or more PLL programming values from the PLL Parameter register.
1	1	0	Command	This 8-bit register selects the color mode, for instance 8-bit Pseudo Color, Hi-Color, True Color, or XGA, and DAC power down. The registers are reset to pseudo color mode on power up.
1	0	1	PLL Parameter	There are sixteen parameter registers as indexed by PLL Address Write/Read registers. Parameter registers 00-0D and 0F are two bytes long and 0E* is one byte long. This register set contains one control register. The bits of this register include clock select and enable functions, the rest contain PLL frequency parameters. After writing the start index address in the PLL address register, these registers can be accessed in successive two (or one) bytes. The address register auto increments after one or two bytes to access the entire register set.

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Absolute Maximum Ratings

Power Supply Voltage .... 7 V

Voltage on any other pin ...... GND – 0.5V to V_{DD} + 0.5V

Temperature under bias .... – 40° C to 85° C

Storage Temperature .... – 65° C to 150° C

DC Digital Output Current .... 25 mA

Analog Output Current .... 45 mA

Reference Current .... –15 mA

Power Dissipation .... 1.0 W

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
DC CHARACTERISTICS (note: J)					
V_{DD}	Positive supply voltage		4.75	5.25	V
V_{IH}	Input logic "1" voltage		2.0	V_{DD} + 0.5	V
V_{IL}	Input logic "0" voltage		– 0.5	0.8	V
I_{REF}	Reference current		–7.0	–10	mA
V_{REF}	Reference voltage		1.10	1.35	V
I_{IN}	Digital input current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 10	μA
I_{OZ}	Off-state digital output current	V_{DD} = max, GND ≤ V_{IN} ≤ V_{DD}		± 50	μA
I_{DD}	Average power supply current	I_O = max, Digital outputs unloaded		250	mA
I_{DACOFF}	DACs in power down mode	No palette access		50	mA
V_{OHS}	Sense logic "1"	I_O = .4mA	2.4		V
V_{OLS}	Sense logic "0"	I_O = .4mA		0.4	V
V_{OHC}	Clock logic "1"	I_O = TBD	2.4		V
V_{OLC}	Clock logic "0"	I_O = TBD		0.4	V
V_{OH}	logic "1"	I_O = -3.2mA, note K	2.4		V
V_{OL}	logic "0"	I_O = 3.2mA, note K		0.4	V
$ICLK_{r}*$	Input Clock Rise Time	TTL levels		15	ns
$ICLK_{f}*$	Input Clock Fall Time	TTL levels		15	ns
F_D	Frequency Change of CLK0 and CLK1 over supply and temperature	With respect to typical frequency		0.05	%

Electrical Characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Units
DAC CHARACTERISTICS (note: J)					
V_O (max)	Maximum output voltage	$I_O \leq 10$ mA		1.5	V
I_O (max)	Maximum output current	$V_O \leq 1$V		21	mA
	Full scale error	note A, B		± 5	%
	DAC to DAC correlation	note B		±2	%
	Integral Linearity, 6-bit	note B		±0.5	LSB
	Integral Linearity, 8-bit	note B		±1	LSB
	Full scale settling time*, 6-bit	note C		28	ns
	Full scale settling time*, 8-bit	note C		20	ns
	Rise time (10% to 90%)*	note C		6	ns
	Glitch energy*	note C		200	pVsec

* Characterized values only

Symbol	Parameter	Conditions	Min	Max	Units
PLL AC CHARACTERISTICS					
f_0	Clock 0 operating range*		25	135	MHz
f_1	Clock 1 operating range*		25	135	MHz
t_r	Output clocks rise time*	25 pf load, TTL levels		3	ns
t_r	Output clocks fall time*	25 pf load, TTL levels		3	ns
d_t	Duty Cycle*		40/60	60/40	%
j_{1s}	Jitter, one sigma*			130 ps	ps
j_{abs}	Jitter, absolute*		-300 ps	300 ps	ps
f_{ref}	Input reference frequency*	Typically 14.318 MHz	5	25	MHz

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AC Electrical Characteristics (note: J)

Symbol	Parameter	Condition	80 MHz Min	80 MHz Max	110 MHz Min	110 MHz Max	135 MHz Min	135 MHz Max	Units
t_{CHCH}	PCLK period		12.5		9.09		7.4		ns
Δt_{CHCH}^*	PCLK jitter	note D		±2.5		+2.5			%
t_{CLCH}	PCLK width low		5		3.6		3		ns
t_{CHCL}	PCLK width high		5		3.6		3		ns
t_{PVCH}	Pixel word setup time	note E	3		3		2		ns
t_{CHPX}	Pixel word hold time	note E	3		2		1		ns
t_{BVCH}	BLANK* setup time	note E	3		3		2		ns
t_{CHBX}	BLANK* hold time	note E	3		2		1		ns
t_{CHAV}^*	PCLK to valid DAC output	note F		20		20		20	ns
Δt_{CHAV}	Differential output delay	note G		2		2		2	ns
t_{WLWH}	WR* pulse width low		50		50		50		ns
t_{RLRH}	RD* pulse width low		50		50		50		ns
t_{SVWL}	Register select setup time	Write cycle	10		10		10		ns
t_{SVRL}	Register select setup time	Read cycle	10		10		10		ns
t_{WLSX}	Register select hold time	Write cycle	10		10		10		ns
t_{RLSX}	Register select hold time	Read cycle	10		10		10		ns
t_{DVWH}	WR* data setup time		10		10		10		ns
t_{WHDX}	WR* data hold time		10		10		10		ns
t_{RLQX}	Output turn-on delay		5		5		5		ns
t_{RLQV}	RD* enable access time			40		40		40	ns
t_{RHQX}	Output hold time		5		5		5		ns
t_{RHQZ}	Output turn-off delay	note H		20		20		20	ns
t_{WHWL1}	Successive write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL1}	WR* followed by read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL1}	Successive read interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHWL1}	RD* followed by write interval	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHWL2}	WR* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{WHRL2}	RD* after color write	note I	4 (t_{CHCH})		4 (t_{CHCH})		4 (t_{CHCH})		cycle
t_{RHRL2}	RD* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{RHWL2}	WR* after color read	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{WHRL3}	RD* after read address write	note I	8 (t_{CHCH})		8 (t_{CHCH})		8 (t_{CHCH})		cycle
t_{SOD}	SENSE* output delay			1		1	1		μs

NOTES:

A. Full scale error is derived from design equation
{[(F.S.I_{OUT}) R_L - 2.1 (I_{REF}) R_L]/[2.1(I_{REF})R_L]} 100%

$V_{BLACK\ LEVEL}$=0V F.S.I_{OUT} = Actual full scale measured output

B. R= 37.5Ω, I_{REF} = - 8.88mA

C. Z_i = 37.5Ω + 30 pF, I_{REF} = - 8.88mA

D. This parameter is the allowed Pixel Clock frequency variation. It does not permit the Pixel Clock period to vary outside the minimum values for Pixel Clock (t_{CHCH}) period.

E. It is required that the color palette's pixel address be a valid logic level with the appropriate setup and hold times at each rising edge of P_{CLK} (this requirement includes the blanking period).

F. The output delay is measured from the 50% point of the rising edge of CLOCK to the valid analog output. A valid analog output is defined when the analog signal is halfway between its successive values.

G. This applies to different analog outputs on the same device.

H. Measured at ± 200 mV from steady state output voltage.

I. This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

J. The following specifications apply for V_{DD} = +5V± 0.5V, GND=0. Operating Temperature = 0°C to 70°C.

K. Except for SENSE pin.

AC Test Conditions

Input pulse levels..V_{DD} to 3V
Input rise and fall times (10% to 90%)..........................3ns
Digital input timing reference level............................1.5V
Digital output timing reference level........0.8V and 2.4V

Capacitance

C_1 Digital input...7pF
C_0 Digital output...7pF
C_{0A} Analog output..10pF

DIGITAL OUTPUT LOAD
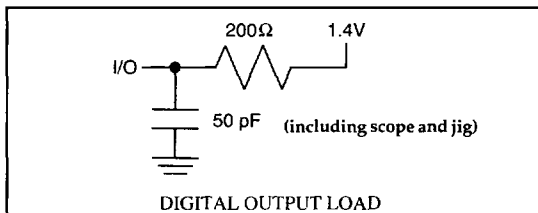
General Operation

The ICS5340 GENDAC is intended for use as the analog output stage of raster scan video systems. It contains a high-speed Random Access Memory of 256 x 18-bit words, three 6/8-bit high-speed DACs, a microprocessor/graphic controller interface, a pixel word mask, on-chip compara-tors, and two user programmable frequency generators.

An externally generated BLANK* signal can be applied to pin 66 of the ICS5340. This signal acts on all three of the analog outputs. The BLANK* signal is delayed internally so that it appears with the correct relationship to the pixel bit stream at the analog outputs.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the color palette RAM to facilitate such operations as animation and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

The ICS5340 also includes dual PLL frequency generators providing a video clock (CLK0) and a memory clock (CLK1), both generated from a single 14.318 MHz crystal. There are eight selectable CLK0 frequencies. Six are programmable, and two are fixed. There are two select-able and programmable CLK1 frequencies (fA, fB). De-fault values (Table 1 and Table 2) are loaded into the appropriate registers on power up.

Video Path

The GENDAC supports nine different video modes and is determined by bits 4-7 of the command register. The default mode is the 8-bit Pseudo Color mode. The other modes are the bypass 15-bit, 16-bit and 24 bit True Color modes in 8-bit and 16-bit interface, and the 16-bit Pseudo Color (2:1) mode with 2X Clock. . The 16-bit True Color has sparse and packed modes.

Pseudo Color

8-bit Interface
In this mode, Pixel Address, P0-P7 and BLANK* inputs are sampled on the rising edge of the clock (PCLK) and any change appears at the analog outputs after three succeeding rising edges of the PCLK. The DAC outputs depends on the data in the color palette RAM.

16-bit Interface
In this mode, Pixel Address, P0-P15 and BLANK* inputs are sampled on the rising edge of the clock (PCLK) and any change appears at the analog outputs after three succeeding rising edges of the 2 x ICLK. The DAC outputs depends on the data in the color palette RAM.

Bypass Mode

The GENDAC supports seven different bypass modes : three for byte transfers and four for word transfers. In these modes, the address pins P0-P15 represent Color Data that is applied directly to the DAC . The internal look-up table RAM is ignored. During byte transfers, the P8-P15 inputs are Don't Care. Data is always latched on the rising edge of PCLK. Byte or Word framing is internally synchronized with the rising edge of BLANK*.

Dac Outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an I_{REF} of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.   The formula for calculating I_{REF} with various peak white voltage/output loading combinations is given below:

$$I_{REF} = \frac{V_{PEAK\,WHITE}}{2.1 \times R_{EFFECTIVE}}$$

Note that for all values of I_{REF} and output loading:

$$V_{BLACK\,LEVEL} = 0$$

The reference current I_{REF} is determined by the reference voltage V_{REF} and the value of the resistor connected to R_{SET} pin. V_{REF} can be the internal band gap reference voltage or can be overridden by an external voltage. In both cases $I_{REF} = V_{REF}/R_{SET}$.
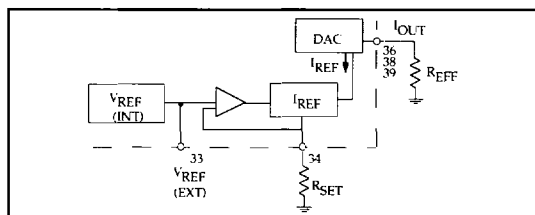

Figure 4 - DAC Set up

The BLANK* input to the GENDAC acts on all three of the DAC outputs. When the BLANK* input is low, the DACs are powered down.

The connection between the DAC outputs of the ICS5340 and the RGB inputs of the monitor should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor.

RF techniques should be observed to ensure good fidelity. The PCB trace connecting the GENDAC to the offboard connector should be sized to form a transmission line of the correct impedance. Correctly matched RF connectors should be used for connection from the PCB to the coaxial cable leading to the monitor and from the cable to the monitor.

There are two recommended methods of DAC termination: double termination and buffered signal. Each is described below with its relative merits:
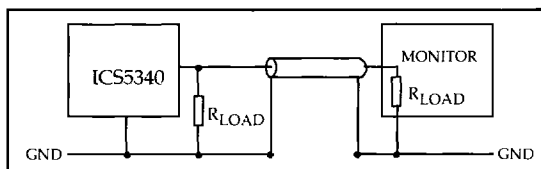
Double Termination (Figure 1)
For this termination scheme, a load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line. Double termination of the DAC output allows both ends of the transmission line between the DAC

outputs and the monitor inputs to be correctly matched. The result should be an ideal reflection free system. This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

A doubly terminated DAC output will rise faster than any singly terminated output because the rise time of the DAC outputs is dependent on the RC time constant of the load.

Figure 1 - Double Termination

Buffered Signal (Figure 2)

If the GENDAC drives large capacitive loads (for instance long cable runs), it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should also be considered as a transmission line. The buffer output will have a relatively low impedance. It should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.
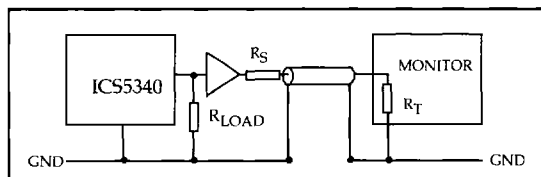
Figure 2 - Buffered Signal

SENSE Output

The GENDAC contains three comparators, one each for the DAC output (R, G and B) lines. The reference voltage to the comparators is proportional to the V_{REF} (internal or external) and is typically 0.33 for V_{REF} =1.23 Volts. When the voltage on any of these pins go higher than the

reference voltage to the comparators, the SENSE* pin is driven low. This signal is used to detect the type of (or lack of) monitor connected to the system.

PLL Clock

The ICS5340 has dual PLL frequency generators for generating the video clock (CLK0) and memory clock (CLK1) needed for graphics subsystems. Both these clocks are generated from a single 14.318 MHz crystal or can be driven by an external clock source. The chip includes the capacitors for the crystal and all the components needed for the PLL loop filters, minimizing board component count.

There are eight possible video clock, CLK0, frequencies (f0-f7) which can be selected by the external pins CS0-CS2. Pins are software selectable by setting a bit in the PLL control register. Two of these frequencies (f0-f1) are fixed and the other six (f2-f7) can be programmed for any frequency by writing appropriate parameter values to the PLL parameter registers. The default frequencies on power up are commonly used video frequencies (table 1). At power up, the frequencies can be selected by pins CS0-CS2. There are two programmable memory clock frequencies (fA, fB). On power up this frequency defaults to the frequency given in table 2. The memory clock transition between frequencies is smooth and glitch free if the transition is kept between the limits 45-65 MHz.

fA	(MHz)	VLCK Comments
f0	25.175	VGA0 (VGA Graphics) (fixed)
f1	28.322	VGA1 (VGA Text) (fixed)
f2	31.500	VESA 640 x 480 @72 Hz (programmable)
f3	36.00	VESA 800 x 600 @56 Hz (programmable)
f4	40.00	VESA 800 x 600 @60 Hz (programmable)
f5	44.889	1024 x 768 @43 Hz Interlaced (programmable)
f6	65.00	1024 x 768 @ 60 Hz, 640 x 480 Hi-Color @ 72 Hz (programmable)
f7	75.00	VESA 1024 x 768 @ 70 Hz, True Color 640 x 480 (programmable)

Table 1 - Video clock (CLK0) default frequency register (with a 14.318 MHz input)

fn	MHz	Comments
fA	45.00 MHz	Memory and GUI subsystem clock
fB	55.00 MHz	Memory and GUI subsystem clock

Table 2 - Memory Clock (CLK1) default frequency register

Microprocessor Interface

Below are listed the six microprocessor interface registers within the ICS5340, and the register addresses through which they can be accessed.

RS2	RS1	RS0	Register Name
0	0	0	Pixel Address (write mode)
0	1	1	Pixel Address (read mode)
0	0	1	Color Value
0	1	0	Pixel Mask
1	0	0	PLL Address (write mode)
1	0	1	PLL Parameter
1	1	0	Command
1	1	1	PLL Address (read mode)
0/HF	1	0	Command Register accessed by (hidden) flag after special sequence of events

Table 3 - Microprocessor Interface Registers

Asynchronous Access to Microprocessor Interface
Accesses to all registers may occur without reference to the high speed timing of the pixel bit stream being processed by the GENDAC. Data transfers between the color palette RAM and the Color Value register, as well as modifications to the Pixel Mask register, are synchronized to the Pixel Clock by internal logic. This is done in the period between microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow the appropriate transfers or modifications to take place. Access to PLL address, PLL parameter and to the command register are asynchronous to the pixel clock.

The contents of the palette RAM can be accessed via the Color Value register and the Pixel Address registers.

Writing to the color palette RAM

To set a new color definition, a value specifying a location in the color palette RAM is first written to the Write mode Pixel Address register. The values for the red, green and blue intensities are then written in succession to the Color Value register. After the blue data is written to the Color Value register, the new color definition is transferred to the RAM, and the Pixel Address register is automatically incremented.

Writing new color definitions to a set of consecutive locations in the RAM is made easy by this auto-incrementing feature. First, the start address of the set of locations is written to the write mode Pixel Address register, followed by the color definition of that location. Since the address is incremented after each color definition is written, the color definition for the next location can be written immediately. Thus, the color definitions for consecutive locations can be written sequentially to the Color Value register without re-writing to the Pixel Address register each time.

Reading from the RAM
To read a color definition, a value specifying the location in the palette RAM to be read is written to the read mode Pixel Address register. After this value has been written, the contents of the location specified are copied to the Color Value register, and the Pixel Address register automatically increments.

The red, green and blue intensity values can be read by a sequence of three reads from the Color Value register. After the blue value has been read, the location in the RAM currently specified by the Pixel Address register is copied to the Color Value register and the Pixel Address again automatically increments. A set of color values in consecutive locations can be read simply by writing the start address of the set to the read mode Pixel Address register and then sequentially reading the color values for each location in the set. Whenever the Pixel Address register is updated, any unfinished color definition read or write is aborted and a new one may begin.

The Pixel Mask Register
The pixel address used to access the RAM through the pixel interface is the result of the bitwise ANDing of the

incoming pixel address and of the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the RAM contents. By partitioning the color definitions by one or more bits in the pixel address, such effects as rapid animation, overlays, and flashing objects can be produced.

The Pixel Mask register is independent of the Pixel Address and Color Value registers.

The Command Register

The Command register is used to select the various GEN-DAC color modes and to set the power down mode. On power up this register defaults to an 6-bit Pseudo Color mode. This register can be accessed by control pins RS2-RS0, or by a special sequence of events for graphics subsystems that do not have the control signal RS2. For graphic systems that do not have RS2, this pin is tied low and an internal flag (HF; Hidden Flag) is set when the pixel mask register is read four times consecutively. Once the flag is set, the following Read or Write to the pixel mask register is directed to the command register. The flag is reset for Read or Write to any register other than the pixel mask register. The sequence has to be repeated for any subsequent access to the command register.

The PLL Parameter Register

The CLK0 and CLK1 of the ICS5340 can be programmed for different frequencies by writing different values to the PLL parameter register bank. There are eight registers in the parameter register; seven are two bytes long and one (0E) is one byte long.

Writing to the PLL parameter register

To write the PLL parameter data, the corresponding address location is first written to the PLL address register. For software compatibility with other chips, two address registers are defined; the Write mode PLL address register and the Read mode PLL address register. They are actually a single Read/Write register in the ICS5340. The next PLL parameter write will be directed to the first byte of the address location specified by the PLL address register. The next Write to the parameter register

will automatically be to the second byte of this register. At the end of the second Write the address is automatically incremented. For the one byte "0E" register the address location is incremented after the first byte Write. If this frequency is selected while programming, the output frequency will change at the end of the second Write.

Reading the PLL parameter register

To read one of the registers of the PLL parameter register the address value corresponding to the location is first written to the PLL address register. The next PLL parameter read will be directed to the first byte of the address location pointed by this index register. A next Read of the parameter register will automatically be the second byte of this register. At the end of the second Read, the address location is automatically incremented. The address register (0E) is incremented after the first byte Read.

Power Down Mode

When bit 0 in the Command register is high (set to 1), the GENDAC enters the DAC power down mode. The DACs are turned off, and the data is retained in the RAM. It is possible to access the RAM, in which case the current will temporarily increase. While the RAM is being accessed, the current consumption will be proportional to the speed of the clock. There is no effect on either clock generator while in this mode.

Power Supply

As a high speed CMOS device, the ICS5340 may draw large transient currents from the power supply, it is necessary to adopt high frequency board layout and power distribution techniques to ensure proper operation of the GENDAC. Please refer to the suggested layout on page 27.

To supply the transient currents required by the ICS5340, the impedance in the decoupling path should be kept to a minimum between the power supply pins V_{DD} and GND. It is recommended that the decoupling capacitance between V_{DD} and GND should be a 0.1µF high frequency capacitor, in parallel with a large tantalum capacitor with

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a value between 22µF and 47µF. A ferrite bead may be added in series with the positive supply to form a low pass filter and further improve the power supply local to the GENDAC. It will also reduce EMI.

The combination of series impedance in the ground supply to the GENDAC, and transients in the current drawn by the device will appear as differences in the GND voltages to the GENDAC and to the digital devices driving it. To minimize this differential ground noise, the impedance in the ground supply between the GENDAC and the digital devices driving it should be minimized.

Digital Output Information

The PCB trace lines between the outputs of the TTL devices driving the GENDAC and the input to the GEN-DAC behave like low impedance transmission lines driven from a low impedance transmission source and terminated with a high impedance. In accordance with transmission line principles, signal transitions will be reflected from the high impedance input to the device. Similarly, signal transitions will be inverted and reflected from the low impedance TTL output. Line termination is recommended to reduce or eliminate the ringing, particularly the undershoot caused by reflections. The termination may either be series or parallel.

Series termination is the recommended technique to use. It has the advantages of drawing no DC current and of using fewer components. Series termination is accomplished by placing a resistor in series with the signal at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and ensures that any signal incident on the TTL output is not reflected.

To minimize reflections, some experimentation will have to be done to find the proper value to use for the series termination. Generally, a value around 100Ω will be required. Since each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. Therefore, the proper value of resistance should be found empirically.

Functional Description

This section describes the register address and bit definition for RAMDAC and the Frequency Synthesizer sections.

Color Palette
Command Register
(RS0-RS2 = 011)
(RS0-RS1 = 01 with hidden flag)

By setting bits in the command register the ICS5340 can be programmed for different color modes and can be powered down for low power operation.

7	6	5	4	3	2	1	0
Color Mode				Reserved = 0			Snooze
2	1	0	3				

Table 3 - Command Registers

Bit 7-4   Color Mode Select
These three bits select the Color Mode of RAMDAC operation as shown in the following table 4 (default is 0 at power up):

Bit 3 - 1   (Reserved)

Bit 0   Power Down Mode of RAMDAC
When this bit is set to 0 (default is 0), the device operates normally. If this bit is set to 1, the power and clock to the Color Palette RAM and DACs are turned off. The data in the Color Palette RAM are still preserved. The CPU can access without loss of data by internal automatic clock start/stop control. The DAC outputs become the same as BLANK* (sync) level output during power down mode. This bit does not effect the PLL clock synthesizer function.

8-BIT INTERFACE						
Mode Number	CM3 (CR4)	CM2 (CR7)	CM1 (CR6)	CM0 (CR5)	Color Mode	Clock Cycles/ Pixel Bits
0	0	0	0	0	8-Bit Pseudo Color with Palette (Default)	1
1	0	0	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
3	0	0	1	0	24-Bit True Color with Bypass (True Color)	3
2	0	0	1	1	16-Bit Direct Color with Bypass (XGA)	2
1	0	1	0	0	15-Bit Direct Color with Bypass (Hi-Color)	2
1	0	1	0	1	15-Bit Direct Color with Bypass (Hi-Color)	2
2	0	1	1	0	16-Bit Direct Color with Bypass (XGA)	2
3	0	1	1	1	24-Bit True Color with Bypass (True Color)	3
16-BIT INTERFACE						
Mode Number	CM3 (CR4)	CM2 (CR7)	CM1 (CR6)	CM0 (CR5)	Color Mode	Clock Cycles/ Pixel Bits
4	1	0	0	0	Muxed 16-Bit Pseudo Color with Palette	1/2
5	1	0	0	1	15-Bit Direct Color with Bypass (Hi-Color)	1
6	1	0	1	0	16-Bit Direct Color with Bypass (XGA)	1
7	1	0	1	1	24-Bit Direct Color with Bypass (True-Color)	2
8	1	1	0	0	24-Bit Packed Direct Color with Bypass (True-Color)	3/2
	1	1	0	1	Reserved	
	1	1	1	0	Reserved	
	1	1	1	1	Reserved	

Table 4 - Color Mode Select

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Color Modes

The nine selectable color modes are described here. Modes 0 - 3 are 8-bit interfaces with P0-P7 bits, P8-P15 are Don't Care bits.

Mode 0: 8-bit Pseudo Color (one clock per pixel). This mode is the 8-bit per pixel Pseudo Color mode. In this mode, inputs P0-P7 are the pixel address for the color palette RAM and are latched on the rising edge of every PCLK. This is the default mode on power up and it is selected by setting bits CR7-CR4 to 0000 . There are three clock cycles pipe line delays from input to DAC output.

8-bit Pseudo Color Mode

PIXEL BYTE							
P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0
PIXEL ADDRESS							

Mode 1: (15-bit per color bypassHi-Color mode).
This mode is the 15-bit per pixel bypass mode. In this mode, inputs P0-P7 are the color DATA and are input directly to the DAC, bypassing the color palette. The two bytes of data is latched in two successive PCLK rising edges. ICS5340 supports only the two clock mode and does not support the mode where the data are latched on the rising and the falling edges. For compatibility, the 15/16 one clock modes are selected as two clock modes in this chip. The low-byte, high byte synchronization is internally done by the rising edge of BLANK*. Each color is 5-bit wide and is packed into two bytes as shown below. This mode can be selected by setting bits CR7-CR4 to 0010, 1000 or 1010.

15-Bit Color Mode 1 Pixel Description
3LSB = set to zero

SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
X	7	6	5	4	3	7	6	5	4	3	7	6	5	4	3
	RED					GREEN					BLUE				

Mode 2: (16-bit per pixel bypass XGA mode).
This mode is the 16-bit per pixel bypass mode and the P0-P7 inputs to go to the DAC directly, bypassing the color palette. The 2 bytes data is latched on two successive rising edges and the low-byte, high-byte synchronization is internally done by the rising edge of BLANK*. In this mode, blue and red colors are 5 bits wide and green is 6 bits wide. The 2 bytes of data is packed as shown below. This mode can be selected by setting bits CR7-CR4 to 0110 or 1100.

16-Bit Color Mode 2 Pixel Description
2LSB = set to zero (green)
3LSB = set to zero (blue, red)

SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7	6	5	4	3	7	6	5	4	3	2	7	6	5	4	3
	RED					GREEN						BLUE			

Mode 3: (24-bit per pixel True Color Mode).
This mode is the 24-bit per pixel bypass mode. The three bytes of data are latched on three successive PCLK edges and the first byte is synchronized by the rising edge of BLANK*. In this mode, each of the colors are 8-bit wide and the DAC is an 8-bit wide DAC. The first byte is blue followed by green and red. This mode can be selected by setting bits CR7-CR4 to 0100 or 1110. The DAC outputs changes every three cycles and the pipeline delay from the first byte to output is five cycles.

24-bit Color Mode 3 Pixel Description

THIRD BYTE								SECOND BYTE								FIRST BYTE							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	RED									GREEN								BLUE					

Modes 4 - 8 use the 16-bit pixel interface.

Mode 4: (8-bit Pseudo Color two pixels per clock) In this mode, inputs P0-P15 are latched on the rising edge of every PCLK. P0-7 and P8-P15 are used for successive addresses for the palette RAM using an internal clock that runs at twice the PCLK frequency. The DAC outputs change twice for every PCLK and the pipeline delay from the first word to output is one and a one half cycles. This mode can be selected by setting bits CR7-CR4 to 0001.

Multiplexed 8-bit Pseudo Color Word Mode 4 Pixel Description

PIXEL WORD															
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	2	0
2nd PIXEL ADDRESS								1st PIXEL ADDRESS							

Mode 5: (16-bit pixel interface, 15-bit per color bypass Hi-Color Mode) In this mode inputs P0-P15 are the color Data and are input directly to the DAC, bypassing the color palette. The Data is latched by the rising edge of PCLK and is pipelined to the DAC. The pipeline delay from input to DAC output is 3 PCLK cycles. Each color is 5-bit wide as shown below. This mode is selected by setting bits CR7-CR4 to 0011.

15-Bit Color Word Mode 5 Pixel Description
3LSB = set to zero

P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	7	6	5	4	3	7	6	5	4	3	7	6	5	4	3
	RED					GREEN					BLUE				

Mode 6: (16-bit pixel interface, 16-bit per color bypass XGA mode) In this mode input P0-P15 are the color Data and are input directly to the DAC bypassing the color Palette. The Data is latched by the rising edge of PCLK and is pipelined to the DAC. The pipeline delay, from input to DAC output, is 3 PCLK cycles. In this mode Blue and Red colors are 5 bits wide, and Green is 6 bits wide. This mode is selected by selecting bits CR7-CR4 to 0101.

16-Bit Color Word Mode 6 Pixel Description
2LSB = set to zero (GREEN)
3LSB = set to zero (BLUE, RED)

P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	7	6	5	4	3	2	7	6	5	4	3
RED					GREEN						BLUE				

Mode 7: (16-bit pixel interface, 24-bit per color bypass TRUE color mode) In this mode inputs P0-P15 are the color Data and are input directly to the DAC bypassing the color Palette. Two words are latched on two successive rising edge of PCLK to form the 24-bit DAC input. The first word and the lower byte of the second word form the 24-bit pixel input to the DAC. The higher byte of the second word is ignored. The low and high word synchronization is internally done by the rising edge of the BLANK*. The pipeline delay from latching of first word to DAC output is 4 cycles and each pixel is 2 pixel clocks wide. In this mode, each of the colors are 8-bits wide and the DAC is 8-bit wide DAC. The first byte is Blue followed by Green and Red. This mode is selected by setting bits CR7-CR4 to 0111.

24-Bit Direct Color Word Mode 7 Pixel Description

FIRST WORD															
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
GREEN								BLUE							

SECOND WORD															
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
								RED							

Mode 8: (16-bit pixel interface packed 24-bit per color bypass TRUE color mode) In this mode inputs P0-P15 are the color Data and are input directly to the DAC bypassing the color Palette. Three words are latched on three successive rising edge of PCLK to form two successive 24-bit DAC inputs. The 16-bit first word and the lower byte of the second word from the first 24-bit pixel input and the second byte of the second word with the 16 bits of the third word from the second 24-bit pixel input. This cycle repeats every 3 cycles. The three word synchronization is internally done by the rising edge of BLANK*. The pipeline delay from latching of first word to DAC output is 3 1/2 cycles and each of the colors are 8-bits wide and DAC is 8-bit wide DAC. The first byte is Blue followed by Green and Red. Repeats. This mode is selected by setting bits CR7-CR4 to 1001.

Packed 24-bit Word Mode 8 Pixel Description
1st DAC Cycle

SECOND WORD								FIRST WORD															
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
			RED								GREEN								BLUE				

2nd DAC Cycle

THIRD WORD																SECOND WORD							
P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
			RED								GREEN								BLUE				

Frequency Generators

The ICS5340 clock synthesizer can be reprogrammed through the microprocessor interface for any set of frequencies. This is done by writing appropriate values to the PLL Parameter Register Bank (table 5).

PLL Address Registers

The address of the parameter register is written to the PLL address registers before accessing the parameter register. This register is accessed by register select pins RS2-RS0 = 100 or 111.

7	6	5	4	3	2	1	0
			PLL REGISTER ADDRESS				
7	6	5	4	3	2	1	0

PLL Parameters Registers

There are sixteen registers in the PLL parameter register (table 5). Registers 00 to 07 are for the CLK0 selectable frequency list, Register 0A for CLK1 programmable frequency and register 0E is the PLL CLK0 control register.

Index	R/W	Register	
00	R/-	CLK0 f0 PLL Parameters	(2 bytes)
01	R/-	CLK0 f1 PLL Parameters	(2 bytes)
02	R/W	CLK0 f2 PLL Parameters	(2 bytes)
03	R/W	CLK0 f3 PLL Parameters	(2 bytes)
04	R/W	CLK0 f4 PLL Parameters	(2 bytes)
05	R/W	CLK0 f5 PLL Parameters	(2 bytes)
06	R/W	CLK0 f6 PLL Parameters	(2 bytes)
07	R/W	CLK0 f7 PLL Parameters	(2 bytes)
08	R/-	(Reserved) = 0	(2 bytes)
09	R/-	(Reserved) = 0	(2 bytes)
0A	R/W	CLK1 fA PLL	(2 bytes)
0B	R/W	CLK1 fB PLL	(2 bytes)
0C	R/-	(Reserved) = 0	(2 bytes)
0D	R/-	(Reserved) = 0	(2 bytes)
0E	R/W	PLL Control Register	(1-byte)
0F	R/-	(Reserved) = 0	(2-byte)

Table 5 - PLL Parameter Registers

PLL CONTROL REGISTER

Bits in this register determine internal or external CLK0 select.

7	6	5	4	3	2	1	0
(RV)	(RV)	ENBL	CLK1	(RV)	INTERNAL SELECT		
=0	=0	INCS	SEL	=0	X	X	X

Bit 7,6, 3 Reserved.

Bit 5 Enable Internal Clock Select (INCS) for CLK0. When this bit is set to 1, the CLK0 output frequency is selected by bit 2 - 0 in this register. External pins CS0 - CS2 are ignored.

Bit 4 Clk1 Select
When this bit is set to 0, fA is selected. When it is set to 1, fB is selected. Default is 0, fA selected, at power up.

Bit 2 - 0 Internal Clock Select for CLK0 (INCS). These three bits selects the CLK0 output frequency if bit 5 of this register is on. They are interpreted as an octal number, n, that selects fn. Default selects f0.

PLL Data Registers

The CLK0 and CLK1 input frequency is determined by the parameter values in this register. These are two bytes registers; the first byte is the M-byte and the second is the N-byte.

M-Byte PLL Parameter Input
The M-byte has a 7-bit value (1-127) which is the feedback divider of the PLL.

7	6	5	4	3	2	1	0
Reserved			M-Divider Value				
=0	X	X	X	X	X	X	X

N-Byte PLL Parameter Input
The N-byte has two values. N1 sets a 5-bit value (1-31) for the input pre scalar and N2 is a 2-bit code for selecting 1, 2, 4, or 8 post divide clock output.

7	6	5	4	3	2	1	0
Reserved	N2-Code		N1-Divider Value				
=0	X	X	X	X	X	X	X

N2 Post Divide Code

If mode 4 is set in the command register, CR7-CR4 equal 0001, N2 code must be 10.

N2 code	Divider
00	1
01	2
10	4
11	8

The block diagram of the PLL clock synthesizer is shown in figure 3.

Based on the M and N values, the output frequency of the clocks is given by the following equation:

$$F_{out} = \frac{(M+2) \times F_{ref}}{(N1+2) \, x2^{N2}}$$

M and N values should be programmed such that the frequency of the VC0 is within the optimum range for duty cycle, jitter and glitch free transition. Optimum duty cycle is achieved by programming N2 for values greater than one. See the next section for programming example.

Programming Example

Suppose an output frequency of 25.175 MHz is desired. The reference crystal is 14.318 MHz. The VCO should be targeted to run in the 100 to 180 MHz range, so choosing a post divide of 4 gives a VCO frequency of :
$$4 \times 25.175 = 101.021 \text{ MHz}$$

From the table in the previous section, we find N2 = 2
Substituting F_{REF} = 14.318 and 2^{N2} = 4 into the equation on page 17:

$$\left(\frac{25.175}{14.318}\right) \cdot 4 = \frac{(M+2)}{(N1+2)}$$

by trial and error:

$$\left(\frac{25.175}{14.318}\right) \cdot 4 \approx \frac{127}{18}$$

so   M + 2 = 127   M = 125
         N1 + 2 = 18   N1 = 16

so the registers are:
    M = 125d = 1 1 1 1 1 0 1 b
    N = 0 & N2 code & N1 = 0 & 1 0 & 1 0 0 0 0
                          N = 0 1 0 1 0 0 0 0 b

Additional Information on Programming the Frequency Generator section of the GENDAC

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When programming the GENDAC PLL parameter registers, there are many possible combinations of parameters which will give the correct output frequency. Some combinations are better than others, however. Here is a method to determine how the registers need to be set:

The key guidelines come from the operation of the phase locked loop, which has the following restrictions:

1. $2 \text{ MHz} < f_{REF} < 32 \text{ MHz}$

    This refers to the input reference frequency. Most users simply connect a 14.318 MHz crystal to the crystal inputs, so this is not a problem.

2. $600 \text{ kHz} < \dfrac{f_{REF}}{(N1+2)} \leq 8 \text{ MHz}$
    This is the frequency input to the phase detector.

3. $60\text{ MHz} \leq \dfrac{(M+2)}{(N1+2)} f_{ref} \leq 270\text{ MHz}$

This is the VCO frequency. In general, the VCO should run as fast as possible, because it has lower jitter at higher frequencies. Also, running the VCO at multiples of the desired frequency allows the use of output divides, which tends to improve the duty cycle.

4. f_{CLK0} and $f_{CLK1} \leq 135\text{ MHz}$

This is the output frequency.

These rules lead to the following procedure for determining the PLL parameters, assuming rules 1 and 4 are satisfied.

A. Determine the value of N2 (either 1, 2, 4 or 8) by selecting the highest value of N2, which satisfies the condition $N2* f_{CLK} \leq 270\text{ MHz}$

B. Calculate $\dfrac{(M+2)}{(N1+2)} = \dfrac{2^{N2} f_{out}}{fref}$

C. Now (M+2) and (N1+2) must be found by trial and error. With a 14.318 MHz reference frequency, there will generally be a small output frequency error due to the resolution limit of (M+2) and (N1+2). For a given frequency tolerance, several different (M+2) and (N1+2) combinations can usually be found.
Usually, a few minutes trying out numbers with a calculator will produce a workable combination. Multiplying possible values of (N1+2) by the desired ratio will indicate approximately the value of M. This method is shown in the example below. A program could be written to try all possible combinations of (M+2) and (N1+2) (3937 possible combinations), discard those outside error band, and select from those remaining by giving preference to ratios which use lower values of (M+2). Lower values of (M+2) and (N1+2) provide better noise rejection in the phase locked loop.

Example: Suppose we are using a 14.318 MHz reference crystal and wish to output a frequency of 66 MHz with an error of no greater than 0.5%. What are the values of the PLL data registers?

A. 66*8 = 528 > 250   VCO speed too high
66*4 = 264 > 250   VCO speed too high
66*2 = 132 < 250   VCO speed OK, N2 = 2, N2 code = 01 from table on page 17 of the data sheet.

B. 132/14.31818 = 9.219
This is the desired frequency multiplication ratio.

C. Setting (N1+2) = 3,4,...12, 13 and performing some simple calculations yields the following table: (Note that N1 cannot be 0).

(N1+2)	(N1+2)*9.219	rounded (=M+2)	Actual Ratio	Percent Error
3	27.657	28	9.33	-1.23
4	36.876	37	9.25	-0.34
5	46.095	46	9.20	0.21
6	55.314	55	9.17	0.57
7	64.533	65	9.29	-0.72
8	73.752	74	9.25	-0.34
9	82.971	83	9.22	-0.03
10	92.19	92	9.20	0.21
11	101.409	101	9.18	0.40
12	110.628	111	9.25	-0.34
13	119.847	120	9.23	-0.13

The ratio 83/9 is closest. Thus (N2+2) = 9; N2=7. (M+2) = 83; M = 81. The M-byte PLL parameter word is simply 81 in binary, plus bit 7 (which must be set to 0), or 01010001. The N-byte PLL parameter word is N2 code (01) concatenated with 5 bits of N2 in binary (00111), or 00100111. Once again, bit 7 must be zero.

We have chosen the combination with the least frequency error, but several other combinations are within the 0.5% tolerance. Because the lowest value of (M+2) offers the best damping, the 37/4 combination will have the best power supply rejection. This results in lower jitter due to external noise.
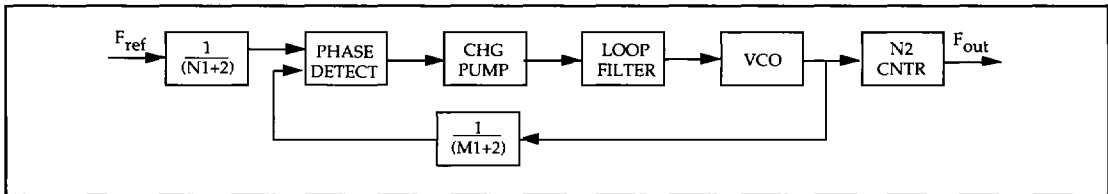
Figure 3 - PLL Clock Synthesizer Block Diagram

External Select			(Internal Select PLL Control Register)			CLK 0 Frequency
CS2	CS1	CS0	BIT 2	BIT 1	BIT 0	
0	0	0	0	0	0	f0
0	0	1	0	0	1	f1
0	1	0	0	1	0	f2
0	1	1	0	1	1	f3
1	0	0	1	0	0	f4
1	0	1	1	0	1	f5
1	1	0	1	1	0	f6
1	1	1	1	1	1	f7

Video Clock Selection Table

System Timing - Pseudo Color, Mode 0

Detailed Timing Specifications - Pseudo Color, Mode 0

System Timing Bypass - 15 (5/5/5) and 16 (5/6/5) Modes 1, 2

System Timing Bypass True Color 24 (8,8,8) Mode 3

System Timing - Multiplexed 8-bit Pseudo Color, Mode 4

System Timing - 16-bit Color, Mode 5 (5,5,5) and 6 (5,6,5)

System Timing - 16-bit Direct True Color, Mode 7

H

System Timing - 24-bit Packed Color, Mode 8

Basic Write Cycle Timing

Basic Read Cycle Timing

Write to Pixel Mask Register Followed by Write

Write to Pixel Mask Register Followed by Read

**Read from Pixel or Pixel Address Register
(Read or Write) followed by Read**

**Read from Pixel or Pixel Address Register
(Read or Write) followed by Write**

Write and Read Back Pixel Address Register (Read Mode)

Write and Read Back Pixel Address Register (Write Mode)

Read Color Value then Pixel Address Register (Read Mode)

Color Value Write followed by any Read

Color Value Write followed by any Write

Color Value Read followed by any Read

Color Value Read followed by any Write

H

Write and Read back PLL Address Register (Write Mode)

Write and Read back PLL Address Register (Read Mode)

Read Two bytes PLL Register then PLL Address Register

Read One Byte PLL Register then PLL Address Register
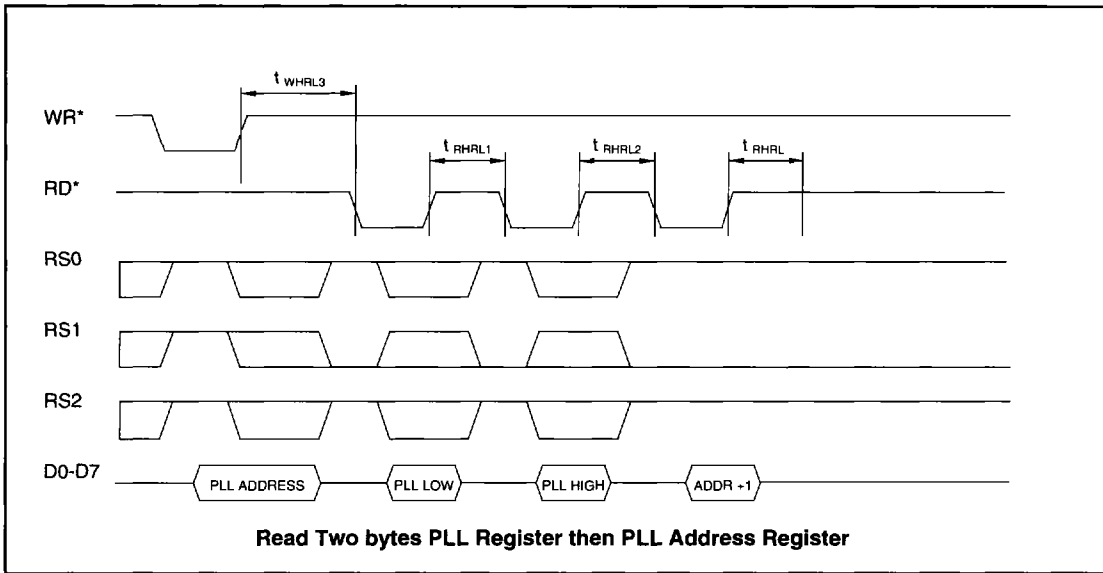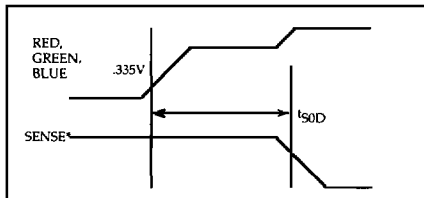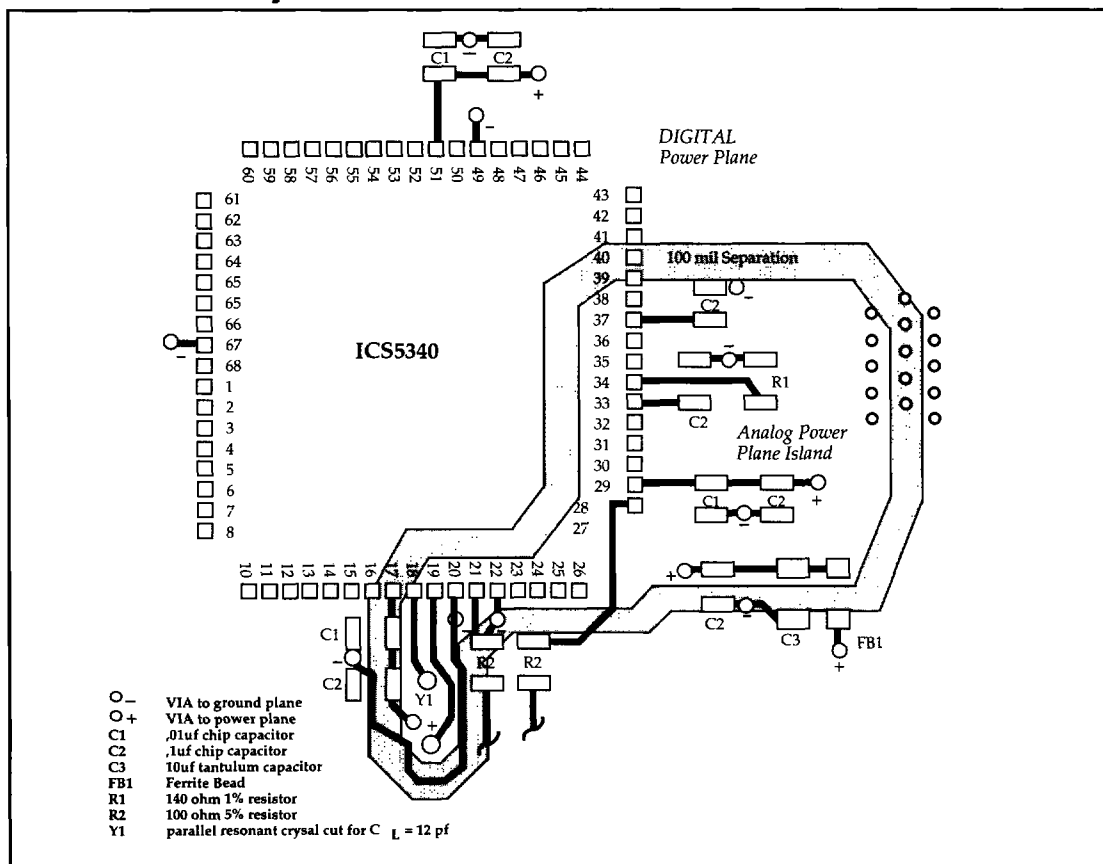
Monitor SENSE Signal

The high performance of which the ICS5340 GENDAC is capable is dependent on careful PC board layout. The use of a four layer board (internal power and ground planes, signals on the two surface layers) is recommended. The layout below shows a suggested configuration.

The ground plane is continuous, but the power plane is separated into analog and digital sections as shown. Power is supplied to the analog power plane through the ferrite bead, and bypassed at the power entry point by C3, a 10 µF tantalum capacitor. These high current connections should have multiple vias to the ground and power planes, if possible. Power connections should be connected to the analog or digital power plane, as shown in the diagram. Power pins 5 and 29 should be connected to digital power, power pins 20 and 24 to analog power. Decoupling capacitors (indicated by C1 and C2) should be placed as close to the GENDAC as possible.

The analog and digital I/O lines are not shown. Analog signals (DAC outputs, Vref, Rset) should only be routed above the analog power plane. Digital signals should only be routed above the digital power plane.

Recommended Layout

O−   VIA to ground plane
O+   VIA to power plane
C1   .01uf chip capacitor
C2   .1uf chip capacitor
C3   10uf tantulum capacitor
FB1   Ferrite Bead
R1   140 ohm 1% resistor
R2   100 ohm 5% resistor
Y1   parallel resonant crysal cut for C$_L$ = 12 pf

Ordering Information

ICS5340V

Example:

ICS XXXX M
- Package Type
  V = PLCC
- Device Type (consists of 3 or 4 digit numbers)
- Prefix
  ICS, AV = Standard Device; GSP = Genlock Device